

Claims

- [c1] We claim, an electrical circuit that provides a cascade switching of power into a multiple load system comprising;
- [c2] A Timer-switch circuit consisting of a timer chip associated with sets of transistor, resistor, diode, and capacitor that activates a double-pole-double-throw relay and with accessible terminals designated as C, D, E, F, and G.
- [c3] A circuit comprising an array of power relays, with one primary relay that provides a common power feeder to a plurality of secondary relays that switch power connection line between factory wiring system and primary relay common power feeder, and with one power relay that bypasses the factory disconnect switch.
- [c4] A Sequential circuit consisting of a multiple flip-flops chip associated with sets of diode, resistor, capacitor, and a chip of power drivers with common positive pin connected to the positive terminal of the dc source through a rectifier diode.
- [c5] A Pulse Generator that generates clock signals supplied to said circuit consisting of a timer chip combined with

resistor, capacitor, and diode sets, that receives sync signals through Sync-sensor and accessible input designated as terminal H.

[c6] A Sync-sensor system comprising a dual op-amp associated with sets of resistor and capacitor with an accessible input designated as terminal K, and with an output connected to said circuit supplying the amplified sync signal.

[c7] The Timer-switch circuit defined in Claim 1 further comprising a power transistor associated with sets of diode and resistor with accessible signal input terminals, designated as A and B, use as paths for passing power-disable signals, and has a direct connection to said circuit sending power-off signal.

[c8] A Deterrent system that suspends and resumes operation of said circuit consisting of a timer chip with associated components of resistor, capacitor, and diode, having means to perform different functions;

–A circuit wherein said means comprises a pair of transistors, wherein first transistor having means to trigger said timer causing second transistor having means applying ground potential to both reset pin of said flip-flops chip in Claim 2 and timer circuit junction in Claim 1.

–A circuit that receives signal through an accessible input designated as J terminal, wherein said first transistor means comprising sets of resistor and diode.

–A circuit with an accessible signal input designated as I terminal, wherein said second transistor means associated with sets of diode and resistor.